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Amendments to the Claims:

This listing of claims will replace all prior version, and listings, of claims in the application. Where claims have been amended and/or canceled, such amendments and/or cancellations are done without prejudice and/or waiver and/or disclaimer to the claimed and/or disclosed subject matter, and the applicant and/or assignee reserves the right to claim this subject matter and/or other disclosed subject matter in a continuing application.

Listing of Claims:

1. (Currently amended) A networking apparatus comprising:

a switching fabric comprising a plurality of ingress/egress points capable of switching routing paths of packets received through mediums coupled to the ingress/egress points; and

a first buffering structure comprising a first plurality of storage structures and a first packet diversion logic and a first packet insertion logic, said first plurality of storage structures comprising an egress diverted packet buffer coupled to said first packet diversion logic and adapted to store diverted ones of egress packets, an egress undiverted packet buffer structurally coupled between the first packet diversion logic and the first packet insertion logic and adapted to store undiverted ones of egress packets, and an egress inserted packet buffer coupled to said first packet insertion logic and adapted to store insertion ones of egress packets, said first buffering structure coupled to a first of said ingress/egress points.

2. (Previously Presented) The apparatus of claim 1, wherein said first buffering structure comprises:

a register interface, including packet unpacking logic, coupled to said egress diverted packet buffer to facilitate retrieval by a processor diverted ones of said egress packets in unpacked portions, wherein the first packet diversion logic is coupled to the first plurality of storage structures and further wherein the first packet diversion logic is capable of selectively routing egress packets from said first ingress/egress point to a selected one of said first plurality of storage structures.

3. (Previously Presented) The apparatus of claim 1, wherein said first buffering structure comprises:

a register interface comprising a packet packing logic capable of facilitating provision to said egress inserted packet buffer by a processor insertion ones of said egress packets in packed portions

wherein the packet insertion logic is coupled to said egress undiverted packet buffer and to said egress inserted packet buffer, wherein the insertion logic is capable of selectively merging undiverted ones and said insertion ones of said egress packets.

4. (Previously Presented) The apparatus of claim 1, further comprising a second buffering structure capable of facilitating a first plurality of ingress packets received from a first medium into said switching fabric through a second of the plurality of ingress/egress points.

5. (Previously Presented) The apparatus of claim 4, wherein said second buffering structure comprises:

a first storage structure capable of staging undiverted ones of said ingress packets;

a second storage structure capable of staging diverted ones of said ingress packets;

a register interface comprising a packet unpacking logic , coupled to the second storage structure, the register interface capable of facilitating retrieval by a processor said diverted ones of said ingress packets in unpacked portions; and

a second packet diversion logic coupled to the first medium and said first and second storage structures of the second buffering structure, wherein the second packet diversion logic is capable of selectively routing said ingress packets received from said first medium onto a selected one of said first and second storage structures of the second buffering structure.

6. (Previously Presented) The apparatus of claim 4, wherein said second buffering

structure comprises:

a first storage structure coupled to said first medium capable of staging undiverted ones of said ingress packets;

a second storage structure capable of staging insertion ones of said ingress packets;

a register interface comprising a packet packing logic capable of facilitating provision to said second storage structure by a processor said insertion ones of said ingress packets in unpacked portions; and

an insertion logic coupled to the first and second storage structures capable of selectively merging said undiverted ones and said insertion ones of said ingress packets.

7. (Previously Presented) The apparatus of claim 4, wherein said second buffering structure is further capable of facilitating at least an additional undiverted one of said ingress packets being received through said second ingress/egress point, and further capable of inserting additional undiverted ones of said ingress packets into said second plurality of ingress packets .

8. (Currently Amended) A networking apparatus comprising:

a switching fabric comprising a plurality of ingress/egress points capable of switching routing paths of packets received through mediums coupled to the ingress/egress points; and

a first buffering structure [[-]]comprising a first plurality of storage structures and a first packet diversion logic and a first packet insertion logic, said first plurality of storage structures comprising an ingress diverted packet buffer coupled to said first packet diversion logic and adapted to store diverted ones of ingress packets, an ingress undiverted packet buffer structurally coupled between the first packet diversion logic and the first packet insertion logic and adapted to store undiverted ones of ingress packets, and an ingress inserted packet buffer coupled to said first packet insertion logic and adapted to store insertion ones of ingress packets, wherein said first buffering structure is coupled to a first of said ingress/egress points.

9. (Previously presented) The apparatus of claim 8, wherein said first buffering structure comprises;

a register interface comprising a packet unpacking logic coupled to said ingress diverted packet buffer, the register interface capable of facilitating retrieval by a processor diverted ones of said ingress packets in unpacked portions, wherein the packet diversion logic is coupled to the first medium and to the first plurality of storage structures, wherein the packet diversion logic is capable of selectively routing ingress packets received from the first medium onto a selected one of said first plurality of storage structures.

10. (Previously Presented) The apparatus of claim 8, wherein said first buffering structure comprises:

a register interface comprising packet packing logic capable of facilitating provision to said ingress inserted packet buffer by a processor insertion ones of said ingress packets in unpacked portions,

wherein the packet insertion logic is coupled to said ingress undiverted packet buffer and to said ingress inserted packet buffer, wherein the packet insertion logic is capable of selectively merging undiverted ones and said insertion ones of said ingress packets.

11. (Currently Amended) A networking apparatus comprising:

a switching fabric including a plurality of ingress/egress points capable of switching packets received through mediums coupled to the ingress/egress points; and

a first buffering structure comprising

a first plurality of storage structures and a first packet diversion logic and a first packet insertion logic, said first plurality of storage structures including an ingress diverted packet buffer coupled to said first packet diversion logic and adapted to store diverted ones of ingress packets, an ingress undiverted packet buffer coupled between the first packet diversion logic and the first packet insertion logic and adapted to store undiverted ones of ingress packets, and an ingress inserted packet buffer coupled to

said first packet insertion logic and adapted to store insertion ones of ingress~~egress~~ packets, said first buffering structure coupled to a first of said ingress/egress points, and

a second buffering structure comprising

a second plurality of storage structures and a second packet diversion logic and a second packet insertion logic, said second plurality of storage structures including an egress diverted packet buffer coupled to said second packet diversion logic and adapted to store diverted ones of egress packets,[[,]] an egress undiverted packet buffer structurally coupled between the second packet diversion logic and the second packet insertion logic and adapted to store undiverted ones of egress packets, and an egress inserted packet buffer coupled to said second packet insertion logic and adapted to store insertion ones of egress packets, said second buffering structure coupled to the first ingress/egress point.

12. (Currently Amended) The apparatus of claim 11, wherein said first plurality of storage structures and associated first packet diversion and insertion logic comprises:

a divert logic coupled to the first ingress/egress point and said ingress undiverted packet buffer and said ingress diverted packet buffer, the divert logic capable of selectively routing said ingress packets from said first ingress/egress point onto a selected one of said ingress undiverted and diverted packet buffers; and

a register interface,[[-]]comprising a packet unpacking logic, coupled to the second storage structure, the register interface capable of facilitating retrieval by a processor diverted ones of said ingress packets in unpacked portions.

13. (Currently Amended) The apparatus of claim 11, wherein said first plurality of storage structures and associated first packet diversion and insertion logic comprises;

a register interface comprising a[[-]]packet packing logic capable of facilitating provision to said ingress inserted packet buffer by a processor insertion ones of said ingress packets in unpacked portions; and

an insertion logic coupled to said egress undiverted packet buffer and to said ingress inserted packet buffer, the insertion logic capable of selectively merging undiverted ones and said insertion ones of said ingress packets.

14. (Previously Presented) The apparatus of claim 11, wherein said second plurality of storage structures and associated second packet diversion and insertion logic comprises;

a first storage structure capable of staging undiverted ones of said egress packets;

a second storage structure capable of staging diverted ones of said egress packets;

a divert logic coupled to a first medium and said first and second storage structures, wherein the divert logic is capable of selectively routing said egress packets received from said first medium onto a selected one of said first and second storage structures; and

a register interface comprising a packet unpacking logic, coupled to the second storage structure, the register interface capable of facilitating retrieval by a processor said diverted ones of said egress packets in unpacked portions.

15. (Previously Presented) The apparatus of claim 11, wherein said second plurality of storage structures and associated second packet diversion and insertion logic comprises;

a first storage structure coupled to a first medium, the first storage structure capable of staging undiverted ones of said egress packets;

a second storage structure capable of staging insertion ones of said egress packets;

a register interface comprising a packet packing logic, wherein the register interface is capable of facilitating provision to said second storage structure by a processor said insertion ones of said egress packets in unpacked portions; and

an insertion logic coupled to the first and second storage structures capable of selectively merging said undiverted ones and said insertion ones of said egress packets.

16. (Currently amended) An optical networking module comprising:

an optical component capable of sending and receiving optical signals encoded with data transmitted through a coupled optical medium;

an optical-electrical component coupled to the optical component capable of encoding digital data onto optical signals and capable of decoding encoded digital data on optical signals back into their digital forms;

a data link/physical layer processing unit, including a buffering structure comprising a plurality of storage structures and a first packet diversion logic and a first packet insertion logic, said plurality of storage structures including an egress diverted packet buffer coupled to said first packet diversion logic and adapted to store diverted ones of egress packets, an egress undiverted packet buffer structurally coupled between the first packet diversion logic and the first packet insertion logic and adapted to store undiverted ones of egress packets, and an egress inserted packet buffer coupled to said first packet insertion logic and adapted to store insertion ones of egress packets, said buffering structure coupled to the optical-electrical component and to a packet source/sink, the buffering structure capable of facilitating at least a selected one of data link/physical processing of ingress packets received from said optical medium for said packet source/sink and egress packets to be routed from said packet source/sink onto said optical medium, wherein each of said data link/physical processing of ingress and egress packets including at least a selected one of diversion of selected ones of a plurality of ingress/egress packets are received from/routed onto said optical medium, and insertion of additional ones into said plurality of ingress/egress packets being received/routed; and

a body encasing said optical component, said optical-electrical component, and said data link/physical processing unit as a single module.

17. (Previously Presented) The optical networking module of claim 16, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises:

a divert logic coupled to said packet source/sink and to said egress undiverted packet buffer and to said egress diverted packet buffer to selectively route said egress packets from said packet source/sink onto a selected one of said egress undiverted

packet and egress diverted packet buffers; and

a register interface, including packet unpacking logic, coupled to said egress diverted packet buffer to facilitate retrieval by a processor diverted ones of said egress packets in unpacked portions.

18. (Previously Presented) The optical networking module of claim 16, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises:

a register interface, including packet packing logic, to facilitate provision to said egress inserted packet buffer by a processor insertion ones of said egress packets in unpacked portions; and

an insertion logic coupled to said egress undiverted packet buffer and to said egress inserted packet buffer to selectively merge undiverted ones and said insertion ones of said egress packets.

19. (Previously Presented) The optical networking module of claim 16, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises:

a first storage structure to stage undiverted ones of said ingress packets;

a second storage structure to stage diverted ones of said ingress packets;

a divert logic coupled to the optical medium and said first and second storage structures to selectively route said ingress packets received from said optical medium onto a selected one of said first and second storage structures; and

a register interface, including packet unpacking logic, coupled to the second storage structure to facilitate retrieval by a processor said diverted ones of said ingress packets in unpacked portions.

20. (Previously Presented) The optical networking module of claim 16, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises:

a first storage structure coupled to the optical medium to stage undiverted ones

of said ingress packets;

a second storage structure to stage insertion ones of said ingress packets;

a register interface, including packet packing logic, to facilitate provision to said second storage structure by a processor said insertion ones of said ingress packets in unpacked portions; and

an insertion logic coupled to the first and second storage structures to selectively merge said undiverted ones and said insertion ones of said ingress packets.

21. (Previously Presented) The optical network module of claim 16, wherein said optical and optical-electrical components and said data link/physical layer processing unit are capable of supporting data rates of at least 10 GB/s.

22. (Previously Presented) The optical network module of claim 16, wherein said data link/physical layer processing unit comprises a multi-protocol processor that is capable of supporting a plurality of datacom and telecom protocols.

23. (Currently amended) A multi-protocol processor comprising:

a plurality of I/O interfaces to facilitate selective optical-electrical trafficking of data transmitted in accordance with a selected one of a plurality of datacom and telecom protocols;

a plurality of data link and physical sub-layer processing units selectively coupled to each other and to the I/O interfaces to be selectively employed in combination to perform selected data link and physical sub-layer processing on egress as well as ingress ones of said data, in accordance with said selected one of said plurality of protocols; and

a buffering structure coupled to at least a system-side one of said I/O interfaces and a media processing one of said data link and physical sub-layer processing units, including a plurality of storage structures and a first packet diversion logic and a first packet insertion logic, said plurality of storage structures including an egress diverted packet buffer coupled to said first packet diversion logic and adapted to store diverted ones of egress packets, an egress undiverted packet buffer structurally coupled

between the first packet diversion logic and the first packet insertion logic and adapted to store undiverted ones of egress packets, and an egress inserted packet buffer coupled to said first packet insertion logic and adapted to store insertion ones of egress packets, said plurality of storage structures to facilitate at least a selected one of diversion of selected ones of a plurality of egress packets, and insertion of additional ones into said plurality of egress packets, diversion of selected ones of a plurality of ingress packets, and insertion of additional ones into said plurality of ingress packets.

24. (Previously Presented) The processor of claim 23, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises:

a divert logic coupled to said packet source/sink and said egress undiverted packet buffer and said egress diverted packet buffer to selectively route said egress packets from said packet source/sink onto a selected one of said egress undiverted packet and egress diverted packet buffers; and

a register interface, including packet unpacking logic, coupled to said egress diverted packet buffer to facilitate retrieval by a processor diverted ones of said egress packets in unpacked portions.

25. (Previously Presented) The processor of claim 23, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises:

a register interface, including packet packing logic, to facilitate provision to said egress inserted packet buffer by a processor insertion ones of said egress packets in unpacked portions; and

an insertion logic coupled to said egress undiverted packet buffer and to said egress inserted packet buffer to selectively merge undiverted ones and said insertion ones of said egress packets.

26. (Previously Presented) The processor of claim 23, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises:

a first storage structure to stage undiverted ones of said ingress packets;

a second storage structure to stage diverted ones of said ingress packets;

a divert logic coupled to the optical medium and said first and second storage structures to selectively route said ingress packets received from said optical medium onto a selected one of said first and second storage structures; and

a register interface, including packet unpacking logic, coupled to the second storage structure to facilitate retrieval by a processor said diverted ones of said ingress packets in unpacked portions.

27. (Previously Presented) The processor of claim 23, wherein said plurality of storage structures and associated packet diversion and insertion logic comprises:

a first storage structure coupled to the optical medium to stage undiverted ones of said ingress packets;

a second storage structure to stage insertion ones of said ingress packets;

a register interface, including packet packing logic, to facilitate provision to said second storage structure by a processor said insertion ones of said ingress packets in unpacked portions; and

an insertion logic coupled to the first and second storage structures to selectively merge said undiverted ones and said insertion ones of said ingress packets.

28. (Previously Presented) The processor of claim 23, wherein said interfaces, said plurality of data link and physical sub-layer processing units and said buffering structure are capable of supporting data rates of at least 10 GB/s.

29. (Original) The processor of claim 23, wherein said processor is disposed on a single integrated circuit.

30. (Currently amended) A buffering structure comprising:

a first storage structure to stage undiverted ones of egress packets, the first storage structure comprising an egress undiverted packet buffer;

a second storage structure to stage diverted ones of egress packets, the second storage structure comprising an egress diverted packet buffer;

a third storage structure to stage insertion ones of egress packets, the third

storage structure comprising an egress inserted packet buffer;

a first divert logic coupled to said first and second storage structures to selectively route egress packets onto a selected exactly one of said first and second storage structures;

a first insert logic coupled to said first and third storage structures to selectively merge said undiverted ones and said insertion ones of said egress packets; and

a register interface, including packet packing and unpacking logic, coupled to the second and third storage structures to facilitate retrieval by a processor said diverted ones of said egress packets in unpacked portions, and provision by said processor said insertion ones of said egress packets in unpacked portions.

31. (Previously Presented) The buffering structure of claim 30, wherein said buffering structure further comprises:

a fourth storage structure to stage undiverted ones of ingress packets;

a fifth storage structure to stage diverted ones of ingress packets;

a second divert logic coupled to said fourth and fifth storage structures to selectively route ingress packets onto a selected one of said fourth and fifth storage structures; and

said register interface, further coupled to the fifth storage structure to facilitate retrieval by said processor said diverted ones of said ingress packets in unpacked portions.

32. (Previously Presented) The buffering structure of claim 30, wherein said buffering structure further comprises:

a fourth storage structure to stage undiverted ones of ingress packets,

a fifth storage structure to stage insertion ones of ingress packets, and

an insertion logic coupled to the fourth and fifth storage structures to selectively merge said undiverted ones and said insertion ones of said ingress packets; and

said register interface further coupled to said fifth storage structure to facilitate provision to said fifth storage structure by said processor said insertion ones of said ingress packets in unpacked portions.

33. (Currently amended) A buffering structure comprising:

a first storage structure to stage undiverted ones of ingress packets, the first storage structure comprising an ingress undiverted packet buffer;

a second storage structure to stage diverted ones of ingress packets, the second storage structure comprising an ingress diverted packet buffer;

a third storage structure to stage insertion ones of ingress packets, the third storage structure comprising an ingress inserted packet buffer;

a first divert logic coupled to said first and second storage structures to selectively route ingress packets onto a selected exactly one of said first and second storage structures;

a first insert logic coupled to said first and third storage structures to selectively merge said undiverted ones and said insertion ones of said ingress packets; and

a register interface, including packet packing and unpacking logic, coupled to the second and third storage structures to facilitate retrieval by a processor said diverted ones of said ingress packets in unpacked portions, and provision by said processor said insertion ones of said ingress packets in unpacked portions.

34. (Previously Presented) The buffering structure of claim 33, wherein said buffering structure further comprises:

a fourth storage structure to stage undiverted ones of egress packets;

a fifth storage structure to stage diverted ones of egress packets;

a second divert logic coupled to said fourth and fifth storage structures to selectively route egress packets onto a selected one of said fourth and fifth storage structures; and

said register interface, also coupled to the fifth storage structure to facilitate retrieval by said processor said diverted ones of said egress packets in unpacked portions.

35. (Previously Presented) The buffering structure of claim 33, wherein said buffering structure further comprises:

a fourth storage structure to stage undiverted ones of egress packets,

a fifth storage structure to stage insertion ones of egress packets, and an insertion logic coupled to the fourth and fifth storage structures to selectively merge said undiverted ones and said insertion ones of said egress packets; and

said register interface is further coupled to said fifth storage structure to facilitate provision to said fifth storage structure by said processor said insertion ones of said egress packets in unpacked portions.

36. (Currently amended) A buffering structure comprising:

a first storage structure to stage undiverted ones of ingress packets, the first storage structure comprising an ingress undiverted packet buffer;

a second storage structure to stage diverted ones of ingress packets, the second storage structure comprising an ingress diverted packet buffer;

a third storage structure to stage undiverted ones of egress packets, the third storage structure comprising an egress undiverted packet buffer;

a fourth storage structure to stage diverted ones of egress packets, the fourth storage structure comprising an egress diverted packet buffer;

a first divert logic coupled to said first and second storage structures to selectively route ingress packets onto a selected exactly one of said first and second storage structures;

a second divert logic coupled to said third and fourth storage structures to selectively route egress packets onto a selected one of said third and fourth storage structures; and

a register interface, including packet unpacking logic, coupled to the second and fourth storage structures to facilitate retrieval by a processor said diverted ones of said ingress and egress packets in unpacked portions.

37. (Previously Presented) The buffering structure of claim 36, wherein said buffering structure further comprises:

a fifth storage structure to stage insertion ones of ingress packets,

an insertion logic coupled to the first and fifth storage structures to selectively

merge said undiverted ones and said insertion ones of said ingress packets; and

said register interface is further coupled to said fifth storage structure to facilitate provision to said fifth storage structure by said processor said insertion ones of said ingress packets in unpacked portions.

38. (Previously Presented) The buffering structure of claim 36, wherein said buffering structure further comprises:

a fifth storage structure to stage insertion ones of egress packets, and

an insertion logic coupled to the third and fifth storage structures to selectively merge said undiverted ones and said insertion ones of said egress packets; and

said register interface is further coupled to said fifth storage structure to facilitate provision to said fifth storage structure by said processor said insertion ones of said egress packets in unpacked portions.

39. (Currently amended) A buffering structure comprising:

a first storage structure to stage undiverted ones of ingress packets, the first storage structure comprising an ingress undiverted packet buffer;

a second storage structure to stage insertion ones of ingress packets, the second storage structure comprising an ingress inserted packet buffer;

a third storage structure to stage undiverted ones of egress packets, the third storage structure comprising an egress undiverted packet buffer;

a fourth storage structure to stage insertion ones of egress packets, the fourth storage structure comprising an egress inserted packet buffer;

a fifth storage structure to stage diverted ones of egress packets;

a divert logic coupled to the third and fifth storage structures to selectively route egress packets onto a selected exactly one of said third and fifth storage structures;

a first insertion logic coupled to the first and second storage structures to selectively merge said undiverted ones and said insertion ones of said ingress packets;

a second insertion logic coupled to the third and fourth storage structures to selectively merge said undiverted ones and said insertion ones of said egress packets; and

a register interface, including packet packing logic, coupled to the second and fourth storage structures to facilitate provision by a processor said insertion ones of said ingress and egress packets in unpacked portions.

40. (Previously Presented) The buffering structure of claim 39, wherein said buffering structure further comprises:

a fifth storage structure to stage diverted ones of ingress packets,

a divert logic coupled to the first and fifth storage structures to selectively route ingress packets onto a selected one of said first and fifth storage structures; and

said register interface is further coupled to said fifth storage structure to facilitate retrieval by said processor said diverted ones of said ingress packets in unpacked portions.

41. (Currently amended) The buffering structure of claim 39, wherein[[,]] ~~said buffering structure further comprises:~~

~~a fifth storage structure to stage diverted ones of egress packets,~~

~~a divert logic coupled to the third and fifth storage structures to selectively route egress packets onto a selected one of said third and fifth storage structures~~;

said register interface is further coupled to said fifth storage structure to facilitate retrieval by said processor said diverted ones of said egress packets in unpacked portions.